REMARKS

The Examiner objected to the drawings and requested that either the drawings or the specification be amended because there was no description of items A and B as found in Figures 2-4. Accordingly, applicants have amended the specification to contain a reference to items A and B as found in the figures.

These references A and B were intended as a reference guide to provide indication of where the flowchart is connected since the flowchart is sufficiently long it cannot fit on a single page. The revisions to the specification clarify such flowchart connections.

Claim 17 was rejected under 35 U.S.C. § 112, second paragraph. Claim 17 has been canceled.

Claims 1-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Roohparvar, U.S. Patent No. 6,587,903. Applicants strongly disagree. The Examiner was of the view that Roohparvar taught performing a first soft-programming row state 244 multiplicity, and provided a reference to columns 5 and 6. Roohparvar does not teach programming a different multiplicity of memory cells. In Roohparvar, the bit line current test is conducted as a verify, to determine whether or not soft-programming is to be conducted at all. It is not conducted to determine the number of memory cells which are to be soft-programmed in a particular programming step. It does not change the number of memory cells which are soft-programmed simultaneously. This will be explained in more detail in the coming paragraphs, which compare to the present invention to Roohparvar.

As explained in the present application, page 8, lines 14-19, the present invention is based on the idea that soft-programming and verifying the memory cells can be a multiplicity, for example, twice, the number which are capable of being programmed using the circuits and their current capability which are present on the device. Indeed, it may well be possible to verify memory cells with a different multiplicity, such as three or four times the number of cells which may be programmed during programming.

According to principles of the present invention, there is a recognition that the number of cells which need soft-programming will be a very small percentage, and substantially less than all of the memory cells. The circuit currently present on the chip can program simultaneously a plurality of memory cells, in the example given, 16 bits. During soft-programming, the goal is correct only those memory cells which are not at the correct erased state. The inventors have recognized that the number of memory cells not at the correct erased stated will be only a small fraction of the total memory cells being addressed. Therefore, a larger number than those cells which can be programmed simultaneously with the current carrying capability of the circuit can be soft-programmed simultaneously. Namely, since it is anticipated that fewer than all of the memory cells, indeed, fewer than half of the memory cells, of the set being verified will need to be programmed that the present invention permits soft-programming a simultaneously of twice or three times as many memory cells as can be programmed during the normal programming operation.

Claim 1 is directed soft-programming and verifying a plurality of memory cells with a multiplicity that is twice (for example 32 bits) that of the one used in programming (for example 16 bits), without any need of supplying from outside the larger current necessary or of increasing the dimensions of the charge pump inside the memory device. Of course, sometimes, the cells needing soft-programming are more than halt the ones selected, therefore the full current capability will be required and the multiplicity will be 1.

This can be obtained in a manner by appropriately modifying the soft-programming algorithm in such a way that it will operate both with the multiplicity used in programming and with a double multiplicity, *i.e.*, twice that used in programming. In particular, in normal operation the soft-programming algorithm operates at double multiplicity (in the example considered, 32 bits), whilst in the case where there is an excessive number of depleted memory cells and it is not possible to soft-program simultaneously the number of memory cells envisaged for double-multiplicity operation because the maximum current required exceeds the capacity of the charge pump, then the soft-programming algorithm passes to operating at single multiplicity, *i.e.*, with the multiplicity used in programming (in an example considered, 16 bits), during which the charge pump is able to supply sufficient current.

After two sets of memory cells (in an example considered, two sets of 16 memory cells each) have been programmed at single multiplicity, the soft-programming algorithm returns to operating at double multiplicity.

Turning now to the prior art, the Examiner has pointed to columns 5 and 6 of Roohparvar '903 patent with respect to soft-programming. The Examiner is correct that Roohparvar '903 describes soft-programming. In fact, the Roohparvar '903 patent is one example of well-known prior art soft-programming techniques of the type described in the specification on pages 1-4 of the application as filed. The similarity ends there. The Examiner points to measuring the current on the bit line in Roohparvar. In the Roohparvar '903 patent, the test carried out in measuring the current is whether or not soft-programming is necessary. This may termed the "verify" step as described in the application and shown in the figures. Namely, as described in column 5, lines 54-62, a verify step is carried out by sensing the current drawn by the bit line when the gate voltage is zero volts. If there is no current drawn, or it is below a predetermined level, then the memory cells are determined to be erased and no soft-programming is carried out. Therefore, the step carried out by Roohparvar is not the soft-programming of the memory cells. Rather, it is the verify step to determine whether or not soft-programming is appropriate. As Roohparvar states in column 5, lines 61-63, if the verify step shows that the bit line current exceeds a certain threshold level, then the memory cells not erased and must be are soft-programmed. Thus, it can be seen that this current draw test is a verify, not the actual carrying out of the soft-programming itself. At the top of column 6, Roohparvar describes the soft-programming being carried out if the verify step fails. In his description, he describes a single memory cell being soft-programmed. He states, in column 6, line 2, that the soft-programming is carried out by biasing "the selected memory cell." Repeatedly through column 6, he refers to "the selected memory cell" and performs testing to determine whether or not the soft-programming has correctly soft-programmed the selected memory cell. In other words, Roohparvar is soft-programming one memory cell at a time. He states in column 6, lines 19-23, that indeed, each memory cell coupled to a bit line is soft-programmed a maximum of one time. He also describes an embodiment in which it is used to soft-program a single memory cell. There is no description in Roohparvar of the number of memory cells which may be soft-

programmed simultaneously in one step being different than the number of memory cells which are soft-programmed in a different step.

According to principles of the present invention, a large plurality of memory cells are soft-programmed simultaneously. In particular, it is known in the programming prior art to program a plurality of memory cells at the same time, for example, 8 bits or 16 bits, all of which may be programmed simultaneously. The number of bits which can be simultaneously programmed is limited by the current drive capability of the programming circuit present on the chip. If more bits are to be programmed simultaneously, a much larger circuit, with larger drive current capability must be provided. The chip designer and manufacturer, therefore, select a maximum number of memory cells which will be programmed simultaneously and provide the appropriate drive current in the circuit. According to principles of the present invention, the soft-programming is carried out as a multiple of the memory cells which the circuit is capable of programming. For example, twice as many memory cells can be soft-programmed as can be programmed in the memory cell. (Alternatively, it may be three or four times as many, depending on the program.)

Turning now to claim 1, claim 1 specifies that a first soft-program is carried out of a first multiplicity of memory cells, for example, twice. Then, a second soft programming is carried out of a different multiple of memory cells, for example, a standard number such as 16 bits which is a different number of bits than was programmed in the first soft-programming step.

The concepts and steps of claim 1 are drastically different than is taught in Roohparvar '903. Roohparvar does not even suggest or hint that a different multiplicity of memory cells may be soft-programmed in different operations. In each of his conditions, he assumes that the same number of memory cells are soft-programmed each time. Indeed, the only description that he provides seems to be that of programming a single memory cells at a time with the soft-programming step. The invention of the Roohparvar '903 patent lies not in increasing the number of memory cells that are soft-programmed simultaneously, but rather, as Roohparvar points out in column 6, beginning at line 38, that the amount of time during which the soft-programming occurs for a given memory cell will be a shorter time period than would be required to program that same memory cell. Thus, Roohparvar takes a completely differently

view and a different approach than that of the present invention. Roohparvar takes the approach of soft-programming the memory cell for a shorter time period than would be required for a programming. Applicants, on the other hand, take the approach of soft-programming a larger number of memory cells simultaneously. For example, two times, or three or four times, the number of memory cells which would normally be programmed simultaneously. Roohparvar, therefore, does not anticipate the present invention and, in fact, completely fails to suggest or even appreciate the approach taken by applicants.

Claim 1 is, therefore, believed patentable over Roohparvar.

A minor typing error was found in claim 1 in that the word "perform" should have been stated "performing," therefore this typing error has been corrected.

Claim 9 is believed patentable over the prior art as originally submitted. Claim 9 specifies means for operating with a first soft-programming multiplicity in given operating conditions and with a second, different soft-programming multiplicity in different operating conditions. This is completely different from and outside the teachings of Roohparvar for the reasons as have been explained.

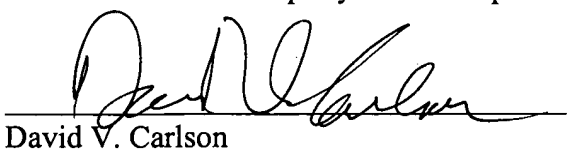
Applicants submit herewith new claims 18-22 which are believed patentable in light of the prior art. Claim 18, as now presented, more particularly points out and distinctly claims applicants' invention, which clearly specifies the sequence of steps of performing a first soft-programming of a first plurality of memory cells simultaneously and then performing a soft-programming of a second plurality of memory cells simultaneously that is fewer than the first plurality of memory cells, if the current drawn during the first programming is higher than a threshold value. Then, a third programming is carried out that is the same number in the plurality of memory cells as the number in the first plurality of memory cells. Claim 18, like claim 1, is also patentably distinct from Roohparvar.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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